What is claimed is:

1. A method of identifying line width errors in an integrated circuit design, comprising:

adding a line width marker for each of a plurality of lines on a schematic, each line having a schematic line width;

assigning a line width parameter to each line width marker;

creating a layout from the schematic, the layout containing the line width markers and a plurality of layout widths;

checking the layout line widths versus the schematic line widths for the plurality of line width marked lines;

creating a design representing the layout, the design having a plurality of design line widths; and

checking the design line widths versus the layout line widths for the plurality of line width marked lines.

2. The method of claim 1, and further comprising excluding from checking the design line widths in areas near or above a transistor.

3. The method of claim 1, wherein checking the layout versus the schematic is performed by layout versus schematic software.

4. The method of claim 1, and further comprising generating an error condition when a design line width is less than a corresponding layout line width.

5. The method of claim 1, and further comprising indicating or recording an error when a design line width is less than a corresponding layout line width.

6. The method of claim 1, wherein creating the layout further comprises drawing the layout as specified by the line width parameters.

7. The method of claim 1, and further comprising generating an error condition when a layout line width is less than a corresponding marked schematic line width.

8. The method of claim 1, and further comprising indicating or recording an error when a layout line width is less than a corresponding marked schematic line width.

9. The method of claim 1, wherein creating a design representing the layout is performed when the all of the layout line widths are greater than or equal to corresponding marked schematic line widths.

10. The method of claim 1, wherein each line width marker and its assigned line width parameter are contained in a line width layer of the layout.

11. A method of identifying line width errors in an integrated circuit design, comprising:

adding a line width marker for each of a plurality of schematic lines on a schematic;

assigning a line width parameter to each line width marker;

creating a first layout from the schematic having a plurality of layout lines, the layout lines respectively corresponding to the schematic lines;

checking the first layout versus the schematic to determine where the layout lines are in the first layout;

creating a second layout including the plurality of layout lines and a width property for each of the layout lines; and

checking the width properties versus the line width parameters.

12. The method of claim 11, and further comprising generating an error condition when a width property is less than a corresponding line width parameter.

13. The method of claim 11, wherein creating a second layout comprises extracting the width properties from the schematic.

14. A method of identifying line width errors in an integrated circuit design, comprising:

adding a line width marker for each of a plurality of schematic lines on a schematic, each schematic line having a schematic line width;

assigning a line width parameter to each line width marker;

creating a layout from the schematic, the layout containing a plurality of layout lines, the layout lines respectively corresponding to the marked schematic lines, each layout line having a layout line width;

determining whether the schematic matches the layout;

transferring the width parameter for each line width marker from the schematic to the layout when the schematic matches the layout;

creating a design representing the layout, the design containing a plurality of design lines, the design lines respectively corresponding to the layout lines, each design line having a design line width;

checking the design line widths versus the corresponding layout line widths; and

generating an error condition when a design line width is less than a corresponding layout line width.

15. The method of claim 14, and further comprising excluding from checking the design line widths in areas near or above a transistor.

16. The method of claim 14, and further comprising indicating or recording the error condition.

17. The method of claim 14, wherein determining whether the schematic matches the layout is performed by layout versus schematic software.

18. The method of claim 14, wherein checking the design line widths versus the corresponding layout line widths is performed by design rule check software.